**Amendments to the Drawings:**

The attached sheet includes changes to Figure 3. This sheet replaces the original sheet.

Attachment

**Remarks/Arguments:**

Claims 1-18 are pending and stand rejected.

By this Amendment, claims 1-2, 8-9, 11-12, 14 and 16-18 are amended and new claim 19 is added. Support for the claim amendments and new claim can be found throughout the original specification and, for example, in the disclosure related to FIGS. 4 and 5 of the original specification.

**Drawing Objections**

In the Office Action, at item 2, the drawings are objected to for FIG. 3 not including a legend such as Prior Art.

Applicants have provided a replacement sheet including FIG. 3 having such a legend.

Reconsideration is respectfully requested.

**Claim Objections**

In the Office Action, at item 3, claims 2, 17 and 18 are objected to because of informalities therein.

Applicants have amended claims 2, 17 and 18 to overcome this objection.

Reconsideration is respectfully requested.

**Rejection of Claim 8 under 35 U.S.C. §112, second paragraph**

In the Office Action, at item 4, claim 8 is rejected under 35 U.S.C. §112, second paragraph as being indefinite.

Applicants have amended claim 8 to overcome the rejection.

Reconsideration is respectfully requested.

**Rejection of Claims 1-3, 5-6, 9 and 16-18 under 35 U.S.C. §102(e)**

In the Office Action, at item 5, claims 1-3, 5-6, 9 and 16-18 are rejected under 35 U.S.C. §102(e) as being anticipated by Kuroda et al. (U.S. Patent No. 6,512,543, hereafter referred to as Kuroda).

Reconsideration is respectfully requested.

Claim 1 is directed to a pixel-capture circuit, and recites:

> a row node carrying a row signal that is operable to couple the node to a column trace during a read period of the captured pixel and operable to set the node to a predetermined signal level during a reset period,
>
> wherein the row signal changes between predetermined voltage levels during at least one portion of the reset period.

**Kuroda Reference**

In the Office Action, at page 4 the Examiner contends that "a row node (a node at line 41 connected to the gate of row select transistor 42) [carries]... a row signal (i.e., Vdd on line 41), that is operable to couple the node to a column trace (43) during a read of the captured pixel and [is] operable to set the node to a predetermined signal level (reset to Vdd level by transistor 60) during a reset phase (see Fig. 3 and col. 8, line 52-col. 9, line 5 and note the timing diagram in Fig. 2)," (brackets added). That is, the Examiner corresponds the row signal of the present invention of claim 1 to the signal on line 41 (i.e., Vdd). More particularly, Kuroda discloses that "in the period 61 during which the nth row is being selected, the row-select-voltage 65 supplied to the selected-row-power-supply line 41 in the nth row becomes HIGH. Therefore, the power supply voltage Vdd is supplied to the power supply input portions of the source follower circuits." (See Kuroda at col. 7, lines 58-63.) Kuroda further discloses that after completion of the output from the pixels arranged in the nth row, a reset voltage 71 applied to the reset voltage input portion 58 is raised from LOW to HIGH in the form of a pulse to form reset pulse 76. (See Kuroda at col. 8, lines 28-31.) That is, during the reset period the photoelectric conversion/storage section 33 is reset to Vdd by the selected-row-power-supply line 41 by turning on pixel reset transistor 60. Thus, in Kuroda throughout the entire reset period, the selected-row-power-supply line 41 (i.e., which the Examiner corresponds to the row node) is maintained at Vdd to supply reset voltage to photoelectric conversion/storage section

33. In particular, the signal is maintained at Vdd during the reset period and is not changed between predetermined levels. This is reinforced in Kuroda, by the reset being enabled by a change in voltage from LOW to HIGH on pixel-reset-voltage-supply line 49. The LOW to HIGH transition of pixel-reset-voltage-supply line 49 is caused by the reset voltage 71 applied to the reset voltage input portion 58 to make the pixel reset transistor conduct. Because reset is based on the pixel-reset-voltage-supply line 49 and not the selected-row-power-supply line 41, the Kuroda circuit structure is different from that recited in claim 1.

Accordingly, it is submitted that claim 1 patentably distinguishes over Kuroda for at least the above set forth reasons.

**Claims 9 and 16**

Claims 9 and 16, which include similar but not identical features to those of claim 1, are submitted to patentably distinguish over Kuroda for at least similar reasons to those of claim 1.

**Claims 2-3, 5-6 and 17-18**

Claims 2-3, 5-6 and 17-18, which include all of the limitations of claim 1 or claim 16, are submitted to patentably distinguish over Kuroda for at least the same reasons as those of claim 1 or claim 16.

**Rejection of Claims 4, 7-8 and 10-15 under 35 U.S.C §103(a)**

In the Office Action, at item 6, claims 4, 7-8 and 10-15 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kuroda in view of Rhodes (U.S. Patent No. 6,812,539).

Reconsideration is respectfully requested.

**Claims 11 and 14**

Claims 11 and 14, which includes similar but not identical features to those of claim 1, are submitted to patentably distinguish over Kuroda for at least similar reasons to those of claims 1.

**Claims 4, 7-8, 10, 12-13 and 15**

Claims 4, 7-8, 10, 12-13 and 15 which include all the limitations of their respective independent claims, are submitted to patentably distinguish over Kuroda for at least the same reasons as their respective independent claims.

**Rhodes Reference**

It is submitted that the addition of Rhodes does not overcome the deficiencies of Kuroda. This is because, Rhodes, which is used by the Examiner to show a two conductive layer configuration with respect to FIG. 13, merely discloses **a convention control mechanism for a 4T circuit**. That is, "an electrical equivalent circuit for the FIG. 1 pixel is illustrated in FIG. 13 of Rhodes with pixel 12 being operated as known in the art by RESET, TRANSFER, and ROW-SELECT signals. Accordingly, Rhodes is silent regarding "the row signal changes between predetermined levels during at least one portion of the reset period," as required by for example claim 1.

Accordingly, it is submitted that claims 4, 7-8, and 10-15 patentably distinguish over the combination of Kuroda and Rhodes, taken singularly or in any proper combination, for at least the above set forth reasons.

**New Claim 19**

New claim 19, which includes all of the limitations of claim 1, is submitted to patentably distinguish over the cited art for at least the same reasons as claim 1.

New claim 19 includes patentable distinctions beyond those of claim 1, namely that: "the row node is coupled to the reset transistor to selectively couple the row node to the node of the pixel capture device for reset and the row node is further coupled to the row selection transistor to control the row selection transistor to selectively couple the node of the pixel capture device to a column trace for readout," as required by claim 19.

Consideration and approval is respectfully requested.

**Conclusion**

In view of the claim amendments, new claim and remarks, Applicants submit the application is in condition for allowance, which action is respectfully requested.

Respectfully submitted,

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JJJ/EB/snp

Dated: May 17, 2007

Enclosure: Replacement sheet for FIG. 3

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The Director is hereby authorized to charge or credit Deposit Account No. **18-0350** for any additional fees, or any underpayment or credit for overpayment in connection herewith.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on:

Stacey Reuss
5/17/07